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Spike Timing Dependent Plasticity with Memristive Synapse in Neuromorphic Systems

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***Abstract*—A methodology to realize spike-timing dependent plasticity and Hebbian learning in a neural network through the usage of memristive synapses is presented. Memristors act as a modulating synapse interconnection between neurons; plasticity is accomplished through adjusting the memristance via current spikes based on the relative timings of pre-synaptic and post-synaptic neuron spikes. The learning plasticity presented is continuous, asynchronous and deterministic. A CMOS implementation is presented along with SPICE simulations validating the methodology and design.**

I. Introduction

Spiking Neural Networks (SNNs) [1]–[3] are time dependent models of biological neural networks. Neurons are modeled with a membrane potential, where the neurons emit spikes when its membrane potential crosses a certain threshold voltage. One popular neuron model is the Leaky-Integrate-and-Fire (LIF) model [1]. Neurons are inter-connected via weighted resistive synapses and thus modulating the relationships between neurons.

A spiking neural network will often employ Hebbian learning [4] and Spike-Timing Dependent Plasticity (STDP) [5] for learning purposes. Hebbian learning dictates that neurons which fire together are deemed correlated and the synaptic strength between those cells should be increased [4]. STDP is a process to adjust the synaptic weights between neurons based on their relative spike timings. Consider the simple scenario where a pre-synaptic neuron is connected via a weighted synapse to a post-synaptic neuron; if the pre-synaptic neuron fires immediately before the post-synaptic neuron firing, the synapse's weight is increased. Contrary, if the pre-synaptic neuron does not fire or fires after the post-synaptic neuron firing, the synapse's weight is decreased.

The memristor was first postulated by Chua in 1971 [6] and first fabricated by Williams at HP in 2008 [7]. The memristor is a fundamental passive two-terminal circuit element. The importance of the memristor is its variable resistance and ability to maintain state passively. Flowing current through a memristor will alter its resistance (memristance), while reversing the current flow will rectify the resistance in the opposite direction. When there is no current flow, the memristor will maintain its state and store its resistance value.

The memristor's abilities to both dynamically adjust its resistance and passive memory capabilities makes it a prime candidate to be used as a synapse connection in a physical neural network implementation. The variable resistance will permit the memristor to learn new synapse weights, while the state abilities will enable the system to remember what it has learned. The concept of using memristors as synapse was first proposed by Snider [8] and have been studied by many researchers since then [9]–[17].

The paper is organized as follows: Section II reviews existing literature and research on the use of memristors as a synapse in a physical neural network system. Section III will state the contributions and novelty this paper introduces. Section IV describes the memristor characteristics and model. Section V briefly reviews spiking neural networks. Section VI expounds the methodology used in this paper. Section VII will present simulation results of the methodology proposed. Section VIII will finish with concluding statements.

II. Related Works

Snider in 2008 first proposed using memristors as synapses in neural network [8]. Snider recognized the memristor's potential in neural networks through its variable memristance; he proposed combining memristor synapses with CMOS neurons to create neuromorphic computing hardware.

Linares-Barranco et al. demonstrated how STDP can be realized via voltage waveforms crossing voltage thresholds regulating memristance. Linares-Barranco also showed how an array of memristors can be interconnected with neurons to be used in a neuromorphic system [10].

Perez et al. extended Linares-Barranco's research exploring methodologies into building memristive synapse neural systems however no circuitry was developed to control the reading and writing of the memristors [11].

Yakopcic et al. presented a read and write logic circuitry for the memristor capable of being updated via neuron spikes, however during reads the memristance levels are discretized into five states. This is non-ideal as one may want to express more than five levels of memristance weight relationships between neurons [12].

TABLE I
DETERMINISTIC, CONTINUOUS AND ASYNCHRONOUS DESIGNS

Contributor	Deterministic	Continuous	Asynchronous
Yakopcic et al. [12]	X		
Cantley et al. [16]		X	X
Ebong et al. [17]	X	X	
Proposed Design	X	X	X

Querlioz et al. demonstrated simulations of a memristor-based spiking neural network immune to device variations; a neural network which could recognize hand written digits from the MNIST [18] database was simulated. Simulations were however done via system C++ code and no physical hardware circuitry was developed [13].

Rose et al. did not focus on STDP but rather on a supervised learning approach for memristor based neural networks. Rose developed a low power CMOS global/local supervised training circuit; a simple neural network learning the "AND" and "OR" boolean logic functions were simulated [14], [15].

Cantley et al. produced a promising circuitry system using nc-Si TFT as a gateway to control current flow across the memristor. The research demonstrated STDP on average when presented with repeated neuron spike correlations or inverse-correlations; however a drawback is that the memristive learning implementation proposed is not deterministic. It is possible for the memristors to consistently learn incorrectly and degrade the neural network's performance which is undesirable and non-ideal [16].

Ebong et al. developed a CMOS circuit demonstrating STDP with continuous learning properties; however the design is synchronous and requires an external synchronous signal [17].

III. CONTRIBUTIONS

This paper contribution is a CMOS circuit design implementing spike spike-timing dependent plasticity with a memristive synapse with:

1) continuous learning memory properties
2) deterministic learning
3) asynchronous operation

Continuous synapse weights are important to permit a smooth range of representable synapse values as opposed to discretized values [12]. Deterministic and predictable plasticity is presented in a learning system as opposed to unguaranteed learning [16]. The design proposed is asynchronous like biological systems as opposed to synchronous designs [17]. Table I gives the summary of this paper's contributions. To the authors' best of knowledge this is the first CMOS circuit design enabling STDP through the usage of memristors that exhibit continuous learning, deterministic learning in an asynchronous form. The CMOS design is also verified via SPICE circuit simulations on the IBM CMOS 180 nm HV process.

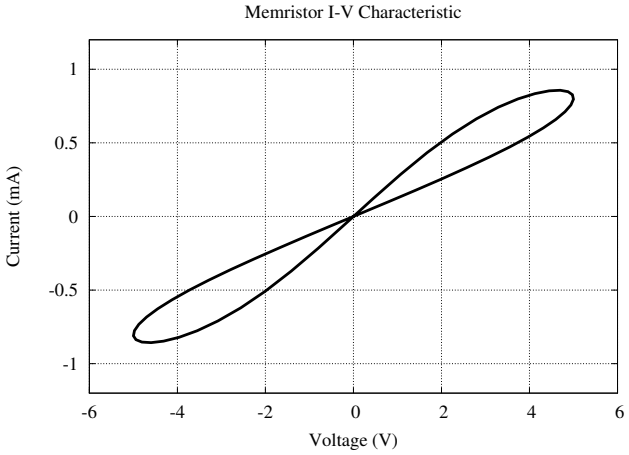

Fig. 1. Memristor Hysteresis I-V Characteristic.

IV. MEMRISTOR MODEL

The memristor was first postulated by Chua in 1971 [6] is a fundamental passive two-terminal element. The memristor with memristance M provides a functional relationship between charge and flux as described by (1):

$$\mathrm{d}\varphi = M\mathrm{d}q \tag{1}$$

More importantly is its consequent relationship between voltage and current described by (2) and its current dependent state equation (3) where w is the state of the memristor:

$$v = R(w,i)i \tag{2}$$

$$\frac{\mathrm{d}w}{\mathrm{d}t} = f(w,i) \tag{3}$$

Intuitively, one can imagine a memristor as a variable resistor where the resistance will increase when current is flowed in one direction; while reversing the current flow will rectify and decrease the resistance. The memristor maintains state, such that when the current is stopped, the memristor will maintain its last known resistance.

Williams at HP [7] in 2008 was the first to fabricate the memristor. The device fabricated was a TiO_2 device. The basic operation of the device is as follows: a thin film of semiconductor (TiO_2) of thickness D is sandwiched between two platinum metal contacts. The semiconductor can be divided into two regions: one with a high concentration of dopants and low resistance (R_{ON}) with width $w(t)$, and the remainder with low dopant concentration and high resistance (R_{OFF}) with width $D - w(t)$.

When an external voltage is applied across the device, the dopants will drift causing a change in size of the high dopant region and low dopant region, and thus a shift in $w(t)$. For the simplest case of linear dopant drift with an average ion mobility μ_v we obtain (4) and (5):

$$v(t) = \left(R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) \quad (4)$$

$$\frac{\mathrm{d}w}{\mathrm{d}t} = \mu_v \frac{R_{ON}}{D} i(t) \quad (5)$$

Biolek has published a SPICE model [19] approximating the operation of the HP TiO_2 memristor device. This SPICE model will be used in the simulations presented below. Fig. 1 gives the I-V characteristic plot of the Biolek memristor fed with a $\pm 5V$ $100Hz$ sine wave; notice the hysteresis loops due to the state conditions.

V. Spiking Neural Networks

The motivation to study Spiking Neural Networks goes beyond the desire to create more accurate models of biological neural networks. Spiking neurons have much more computational power than sigmoidal neurons and also incorporate a time factor permitting temporal learning which is not possible with the latter [20].

A. CMOS Spiking Neuron

Biological neurons emit spikes when their cell membrane potential is reached. Fig. 2 is a variation of the classical Axon-Hillock CMOS neuron [1] which models the behaviour of biological spiking neurons. From the input i, the neuron *integrates* current into a stored charge on its capacitor C_{m0}. If the sufficient threshold voltage potential is built up by the capacitor at the i node (i.e. $^{VDD}/_{2}$), the buffer will drive the output o towards VDD. When the output o crosses the NMOS V_t, the N_{reset} NMOS will be turned on and starts discharging the capacitor C_{m0} which eventually drops the i voltage potential to below the threshold voltage.

This results in a "spiking" neuron: the neuron fires a spike when its threshold voltage is reached and resets itself. The neuron is *leaky* in which it will slowly discharge the capacitor C_{m0} via R_{l0}. This is known as the Leaky-Integrate-and-Fire (LIF) neuron model [1].

B. Spike-Timing Dependent Plasticity

Spike-Timing Dependent Plasticity is a biological process that adjusts the strength of connections between neurons in a biological neural network [5]. The synaptic weights between neurons are adjusted based on the relative spike timings between the pre-synaptic and post-synaptic neurons.

Hebbian learning dictates that when one neuron fires and the other doesn't fire, the synaptic weight between them should decrease. STDP takes this further in the situation where both neurons fire: if the post-synaptic neuron fires after the pre-synaptic neuron fires, the synaptic weight is increased. However, if the post-synaptic neuron fires before the pre-synaptic neuron fires, the synaptic weight is decreased. The scalar quantity of synaptic weight change is dependent on the relative timings of the spikes.

VI. Methodology

A. Neuron Spike Memory

To enable STDP, the system must be able to recognize if a neuron has been recently activated. A "Neuron Spike Memory" circuitry (Fig. 3) was designed to "remember" if a neuron has recently spiked. Each neuron will have one of these Neuron Spike Memory circuitry associated with it to establish whether it has recently been excited. The $\overline{o}$ from Fig. 2 is fed to the $\overline{o}$ from Fig. 3.

Referring to Fig. 3, when the neuron fires, $\overline{o}$ is driven low and thus turning on $P2$. $P2$ acts as a pull up transistor and charges C_{m1}. At the point where C_{m1} crosses the threshold voltage (i.e. $^{VDD}/_{2}$), the inverter chain $P3$, $N3$ and $P4$, $N4$ will drive $\overline{s}$ and s towards VSS and VDD respectively.

When the neuron has finished spiking, $\overline{o}$ is driven high and turns off $P2$. The voltage potential at C_{m1} remains until R_{l1} slowly leaks away the charge. Until the voltage potential at C_{m1} falls below the threshold voltage, the preceding inverter chain will continue driving their respective s and $\overline{s}$ outputs. An important attribute of the Neuron Spike Memory is its memory retention time– or how far into the future will it remember a spike until R_{l1} leaks away the charge.

B. Synaptic Control Circuit

The Synaptic Control Circuit (Fig. 4) connects the pre-synaptic neuron with the post synaptic-neuron and enables STDP. Two important tasks are accomplished; first it regulates current flowing from the pre-synaptic neuron to the post-synaptic neuron and secondly, based on pre-synaptic and post-synaptic neuron spikes, it controls the directional current flow through the memristor M_1 thus implementing STDP.

We use the convention that when current flows "forward" across the memristor it is assumed from left to right and the memristance is increased; the opposite holds true.

1) Pre-Synaptic Neuron Excitation: In the pre-synaptic neuron excitation scenario, the pre-synaptic neuron fires while the post-synaptic neuron is suppressed. Referring to Fig. 4, $P5$, $P6$, $P11$ and $N11$ will be turned on, while the rest of the transistors will be turned off. This creates a current path from VDD via $P5$/$P6$ through the memristor M_1 *forward* to the post-synaptic neuron's input i_{post}. The current will be modulated by the memristor before reaching the post-synaptic neuron (i.e. the memristor's memristance acts as a weight in the neural network). The forward flow of current through the memristor M_1 will also result in an increase in resistance. This is desired due to the Hebbian learning rule; weights should decrease (i.e. resistance should increase) when only one of the neuron is firing.

2) Post-Synaptic Neuron Excitation: In the post-synaptic neuron excitation scenario, the post-synaptic neuron fires while the pre-synaptic neuron remains unexcited. $P7$, $P8$, $N9$, $N10$ will be turned on, while the rest of the transistors will be turned off. This creates a forward current path from VDD via $P7$/$P8$ through the memristor M_1 to VSS via $N9$/$N10$; thus increasing the memristor's memristance as desired. No current

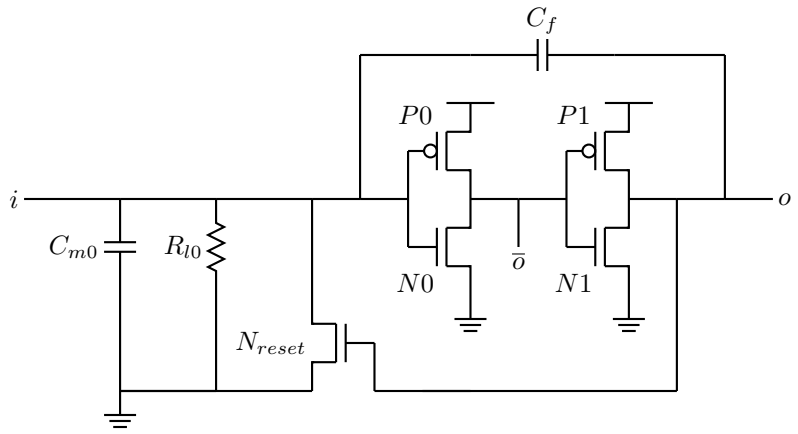

Fig. 2. Leaky-Integrate-and-Fire CMOS Neuron: Classical CMOS neuron firing spikes when its input threshold voltage potential is reached.

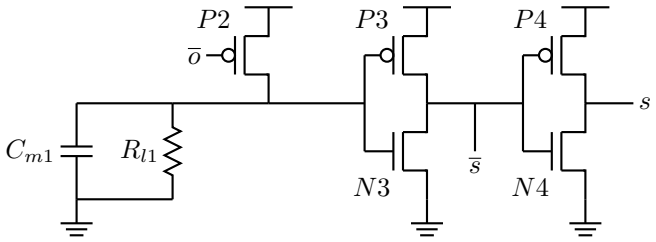

Fig. 3. Neuron Spike Memory: When a neuron fires, C_{m1} charges up remembering its excitation, R_{l1} slowly leaks away the charge and thus determining the memory spike retention time.

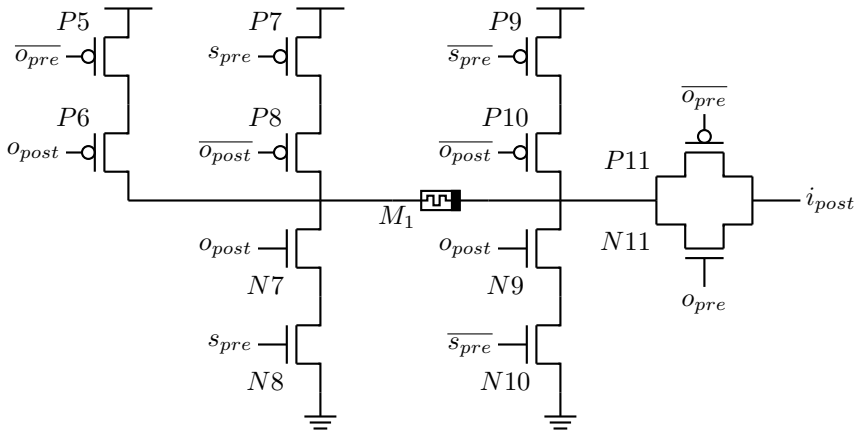

Fig. 4. Synaptic Control Circuit: The M_1 memristor's current flow is regulated based on the spike timings of the pre-synaptic and post-synaptic neurons.

flows into the post-synaptic neuron since the $P11/N11$ MUX is turned off.

3) Pre-Synaptic Neuron then Post-Synaptic Neuron Firing: In this scenario, first the pre-synaptic neuron fires then followed by the post-synaptic neuron firing. There are two stages in the process. In the first stage when the pre-synaptic neuron fires, similar to the Section VI-B1 $P5$, $P6$, $P11$ and $N11$ are on allowing current to flow forward through the memristor M_1 into the post-synaptic neuron's input. However, as soon as the post-synaptic neuron is fired, the second stage begins. $P5$ and $P6$ are turned off halting this the current path. $P9$, $P10$, $N7$ and $N8$ are turned on reversing the current and flowing backwards through memristor, thus decreasing the memristance. As long as the pre-synaptic neuron is still firing, $P11$ and $N11$ are still turned on thus allowing current to still flow into the post-synaptic neuron as desired. $P9$, $P10$, $N7$ and $N8$ remains on until the post-synaptic neuron stops firing or the pre-synaptic neuron's spiked memory s exceeds its memory retention duration.

There are two points to note: first, the net current flow across the memristor allows the memristance to decrease (i.e. there is more current flowing backwards than forwards). The amount the memristance decreases is dependent on the *spike timing*. Secondly, if the post-synaptic neuron fires immediately after

the pre-synaptic neuron, only a small amount of current will flow forwards; however if there is a big delay between the pre-synaptic and post-synaptic spikes, the net memristance delta effect of the current flowing backwards is reduced since it has to first overcome the memristance increase in the first stage. If the delay between pre-synaptic and post-synaptic spikes exceeds the pre-synaptic neuron's spiked memory retention period, the pre-synaptic excitation will no longer be registered. This results in no backward current flow and will be treated exactly as the same as the Pre-Synaptic Neuron Excitation scenario in Section VI-B1.

4) Post-Synaptic Neuron Firing then Pre-Synaptic Neuron: In this scenario, first the post-synaptic neuron fires then followed by the pre-synaptic neuron firing. There are two stages in the process. In the first stage when the post-synaptic neuron fires, $P7$, $P8$, $N9$, and $N10$ will be turned on similar to the Post-Synaptic Neuron Excitation scenario in Section VI-B2 and current will flow forward across the memristor increasing its memristance. The second stage begins when the pre-synaptic neuron fires as well, the $P11/N11$ will then turn on permitting current flow into the post-synaptic neuron's input i_{post} as desired.

If there is an overlap between the post-synaptic and pre-synaptic neuron firing, $P7$, $P8$, $N9$, and $N10$ will be turned off while $P9$, $P10$, $N7$ and $N8$ will turn on. This will result in a current flow backwards decreasing the memristance; this is desired due to Hebbian learning dictating that when two neurons fire together the synaptic weights should increase.

VII. Simulation

Simulations were performed with PSPICE (version 16.5) with an approximated HP TiO_2 memristor model [19] and the IBM 180 nm HV (High Voltage) transistor model. The default memristor parameters were used in the simulation: $R_{ON} = 100\Omega$, $R_{OFF} = 16\text{K}\Omega$, $D = 10\text{nm}$, μ_v=$10^{-14}\text{m}^2\text{V}^{-1}\text{s}^{-1}$ and $p = 10$ for the window function of the nonlinear model [19]. The IBM 180 nm HV process supports high VDD (up to 50V); a high voltage is needed to change the memristor's memristance meaningfully due to its low dopant mobility. The supply voltage was set as $VDD = 10\text{V}$.

PMOS transistors $P0$, $P1$, $P2$, $P3$, $P4$ and $P11$ are sized at $L = 180\text{nm}$ and $W = 2000\text{nm}$; $P5$, $P6$, $P7$, $P8$, $P9$, $P10$ are sized at $L = 180\text{nm}$ and $W = 4000\text{nm}$. NMOS transistors N_{reset}, $N0$, $N1$, $N3$, $N4$, and $N11$ are sized at $L = 180\text{nm}$ and $W = 1000\text{nm}$; $N7$, $N8$, $N9$, $N10$ are sized at $L = 180\text{nm}$ and $W = 2000\text{nm}$. Capacitors C_f, C_{m0} and C_{m1} have capacitance $C = 1\text{uF}$. Resistors R_{l0} and R_{l1} have resistance $R = 50\text{K}\Omega$.

A. Single Neuron Firing

Fig. 5 gives the simulation results where the pre-synaptic neuron is excited while the post-synaptic neuron is suppressed as described in Section VI-B1; Fig. 6 gives the simulation results where the post-synaptic neuron is excited while the pre-synaptic neuron is suppressed as described in Section VI-B2. In both scenarios, the solo neuron is fed with a pulsed input current source with 2mA amplitude, 100ms period and 1µs rise time. In the pre-synaptic firing scenario, the post-synaptic neuron's output o_{post} was pulled to VSS via a low impedance resistor. In the post-synaptic firing scenario, the pre-synaptic neuron's input i_{pre} was connected to VSS.

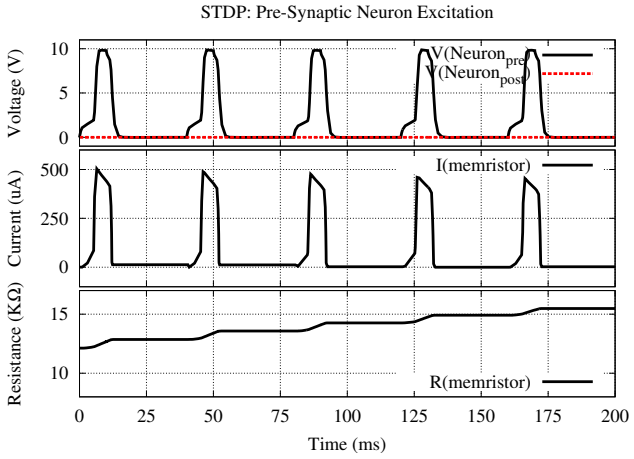

Fig. 5. Simulation: pre-synaptic neuron is excited while the post-synaptic neuron is suppressed; the memristor synaptic weight exhibits an increase in resistance.

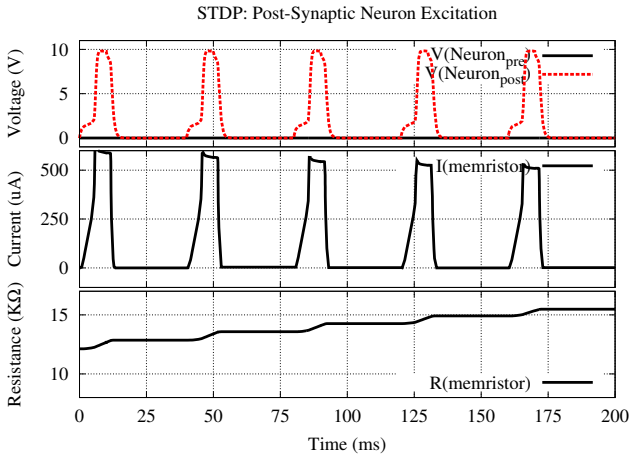

Fig. 6. Simulation: pre-synaptic neuron is suppressed while the post-synaptic neuron is excited; the memristor synaptic weight exhibits an increase in resistance.

As expected, resistance increases with each single neuron firing. Notice learning is non-linear, each subsequent current pulse caused by the solo neuron firing decreases in peak amplitude; this is due the non-linearity of the memristor device.

B. Spike-Timing Dependent Plasticity

Fig. 7 gives the simulation results where both the pre-synaptic and post-synaptic neurons fire. Both neurons were triggered to fire via a single current pulse with 2mA amplitude, 10ms period and 1µs rise time. The post-synaptic neuron's firing relative timing is shifted by Δt; for example when Δt is negative the post-synaptic neuron fires first before the pre-

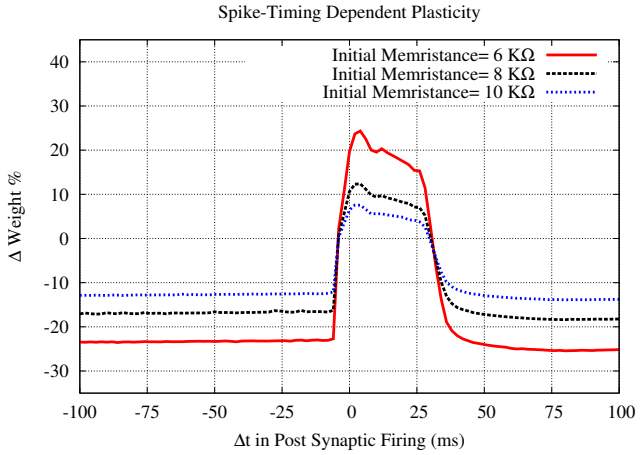

Fig. 7. Simulation: both the pre-synaptic and post-synaptic neurons are excited; the memristor synaptic weight exhibits an increase or decrease in its weight (conductance) dependent on the relative spike timing Δt.

synaptic neuron, and when Δt is positive the pre-synaptic neuron fires first.

Fig. 7 depicts spike-timing dependent plasticity; if the post-synaptic neuron fires before the pre-synaptic neuron the memristance is increased (i.e. weight decreased). When the post-synaptic neuron fires after the pre-synaptic neuron; the memristance is decreased.

In the region $0\text{ms} < \Delta t < 30\text{ms}$, the post-synaptic neuron fires after the pre-synaptic neuron, note the slope indicating a semi-linear plasticity learning in this region. At approximately $\Delta t = 30\text{ms}$, the plasticity slope drastically changes; this is due to the pre-synaptic neuron's spike memory s_{pre} losing its memory potential. For a small duration where the post-synaptic neuron fires before the pre-synaptic neuron (approximately $-5\text{ms} < \Delta t < 0\text{ms}$) the memristance decreases; this is where the post-synaptic neuron and pre-synaptic neuron have a period of overlap in their excitation and thus a memristance decrease as expected.

VIII. Conclusion

In conclusion, we have presented a novel CMOS circuit design demonstrating spike-timing dependent plasticity with memristive synapse. STDP is enabled through the relative spike timings of the pre-synaptic and post-synaptic neurons. The plasticity is non-linear, continuous, asynchronous and deterministic. SPICE simulations were performed to validate the design.

The design has some shortcomings in which we require 13 transistors per memristor synapse. The authors believe this is a reasonable area trade-off cost for a design which captures continuous, asynchronous and deterministic plasticity. It should however be noted, due to the low mobility of the simulated device used, in the current design the majority of the area is actually consumed by the capacitors and not the transistors. In future research work, it is aimed to reduce the number of transistors per memristor.

It would be desirable to also replace the TiO_2 memristor device with the Tantalum Oxide (TaOx) memristor device which has much higher switching speeds [21]. The higher speeds will enable the usage of a lower VDD and smaller capacitors which will result in faster spiking speeds, lower power consumption and increased neural density.

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